

Program: Electronics & Telecommunication Engineering
Curriculum Scheme: Rev2016
Examination: Second Year Semester III
Course Code: ECC303 and Course Name: Digital System Design

Time: 1 hour

Max. Marks: 50

For the students:- All the Questions are compulsory and carry equal marks .

Q1.	A product term containing all K variables of the function in either complemented or uncomplemented form is called a _____
Option A:	Minterm
Option B:	Maxterm
Option C:	Least term
Option D:	Midterm
Q2.	The prime implicant which has at least one element that is not present in any other implicant is known as _____
Option A:	Essential prime implicant
Option B:	Implicant
Option C:	Complement
Option D:	Prime complement
Q3.	In case of an OR gate, no matter what the number of inputs a
Option A:	1 at any input causes the output to be at logic 1
Option B:	1 at any input causes the output to be at logic 0
Option C:	0 at any input causes the output to be at logic 1
Option D:	0 at any input causes the output to be at logic 0
Q4.	Which is the correct order of sequence for representing input values in K map
Option A:	00, 01, 10, 11
Option B:	00, 01, 11, 10
Option C:	00, 10, 11, 01
Option D:	00, 10, 01, 11
Q5.	2's complement of binary number 1101 is
Option A:	1011
Option B:	0011
Option C:	0010
Option D:	1110
Q6.	If the functions w, x, y, z are as follows $w = R + \overline{P}Q + \overline{R}S$, $x = PQR\overline{S} + PQR\overline{S} + P\overline{Q}\overline{R}\overline{S}$ $y = RS + \overline{PR + P\overline{Q} + \overline{P}\overline{Q}}$ $z = R + S + \overline{PQ + \overline{P}\overline{Q}} \cdot \overline{R} + P\overline{Q} \cdot \overline{S}$
Option A:	w=z x=z
Option B:	w=z x=y

Option C:	w=y
Option D:	w=y=z
Q7.	For the minterm designation $Y = \sum m (1, 3, 5, 7)$ the complete expression is
Option A:	$Y = \bar{A} \bar{B} C + A \bar{B} C$
Option B:	$Y = \bar{A} \bar{B} C + A \bar{B} C + ABC + \bar{A} BC$
Option C:	$Y = \bar{A} \bar{B} \bar{C} + \bar{A} \bar{B} C + \bar{A} BC + A \bar{B} C$
Option D:	$Y = \bar{A} \bar{B} \bar{C} + ABC + \bar{A} \bar{B} C + A \bar{B} C$
Q8.	BCD code for a decimal number 874 is
Option A:	1000 0111 0100
Option B:	1000 0011 0110
Option C:	1000 0011 0100
Option D:	1000 0111 0110
Q9.	The hexadecimal number 68.4B can be converted to equivalent octal number which is represented as
Option A:	150.226
Option B:	140.226
Option C:	150.116
Option D:	140.116
Q10.	Which logic family provide minimum power dissipation
Option A:	TTL
Option B:	CMOS
Option C:	ECL
Option D:	JFET
Q11.	The dual expression of $x+x.y$ is
Option A:	$x.(x+y)$
Option B:	$x.(x.y)$
Option C:	$x+x+y$
Option D:	$x+x.y$
Q12.	A master slave configuration consists of two identical flip flops connected in a such a way that the output of the master is input to the slave. Which one of the following is correct?
Option A:	Master is level triggered and the slave is edge triggered
Option B:	Master is edge triggered and the slave is level triggered
Option C:	Master is positive edge triggered and the slave is negative edge triggered
Option D:	Master is negative edge triggered and the slave is positive edge triggered
Q13.	In a J-K flipflop, the output Q_n is 1 and it does not change when a clock pulse is applied. The possible combination of J_n and K_n could be (X denotes don't care)
Option A:	X and 1

Option B:	X and 0
Option C:	0 and X
Option D:	1 and X
Q14.	Which of the following VHDL design units contain the description of the circuit?
Option A:	Configurations
Option B:	Architecture
Option C:	Library
Option D:	Entity
Q15.	EPROM is
Option A:	UV light erasable and electrically programmable
Option B:	infrared light erasable and magnetically programable
Option C:	electrostatically erasable and magnetically programmable
Option D:	magnetically erasable and electrically programmable
Q16.	The difference between a PLA and a PAL is
Option A:	the PAL has a programmable OR plane and a programmable AND plane, while the PLA only has a programmable AND plane
Option B:	the PLA has a programmable OR plane and a programmable AND plane, while the PAL only has a programmable AND plane
Option C:	the PAL has more possible product terms than the PLA
Option D:	PALs and PLAs are the same thing.
Q17.	The bit sequence 0111 is serially entered (right-most bit first) into a 4-bit parallel out shift register that is initially clear. What are the Q outputs after two clock pulses?
Option A:	0000
Option B:	1100
Option C:	1000
Option D:	1110
Q18.	A logic circuit that accepts several data inputs and allows only one of them at a time to get through to the output is called
Option A:	Multiplexer
Option B:	Demultiplexer
Option C:	Transmitter
Option D:	Receiver
Q19.	The number of flip-flops required to construct an 8-bit shift register will be
Option A:	32
Option B:	16
Option C:	8
Option D:	4
Q20.	The output in a Mealy machine depends on
Option A:	State
Option B:	Previous state

Option C:	state and input
Option D:	Only input
Q21.	If the output of two-bit asynchronous binary up counter using T flip flops is '00' at reset condition, then what output will be generated after the fourth negative clock edge?
Option A:	10
Option B:	11
Option C:	00
Option D:	01
Q22.	An half adder can be constructed using
Option A:	One XOR gate and one OR gate with their inputs connected in parallel
Option B:	One XOR gate and one OR gate with their inputs connected in series
Option C:	One XOR gate and one AND gate
Option D:	Two XNOR gates only
Q23.	Which of the following memories can be programmed once by the user and then cannot be erased and reprogrammed
Option A:	ROM
Option B:	PROM
Option C:	EPROM
Option D:	EEPROM
Q24.	Which of the following describes the structure of a VHDL code correctly?
Option A:	Library Declaration; Configuration; Entity Declaration; Architecture Declaration
Option B:	Library Declaration; Entity Declaration; Architecture Declaration; Configurations
Option C:	Library Declaration; Entity Declaration; Configuration; Architecture Declaration
Option D:	Library Declaration; Configuration; Architecture Declaration; Entity Declaration
Q25.	What is the addition of the binary numbers 10011011010 and 010100101?
Option A:	0111001000
Option B:	1100110110
Option C:	10101111111
Option D:	10011010011