Program: BE Information Technology

Curriculum Scheme: Revised 2016

Examination: Third Year Semester VI

Course Code: ITC404 and Course Name: COA

Time: 1hour Max. Marks: 50

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Note to the students:- All the Questions are compulsory and carry equal marks .

Q1.	The size of each segment in 8086 is
Option A:	64 kb
Option B:	24 kb
Option C:	50 kb
Option D:	16kb
Q2.	In 8086 the overflow flag is set when_____.
Option A:	The sum is more than 16 bit
Option B:	Carry and sign flags are set
Option C:	Signed numbers go out of their range after an arithmetic operation
Option D:	During subtraction
Q3.	The method of accessing the I/O devices by repeatedly checking the status flags is
Option A:	Program-controlled I/O
Option B:	Memory-mapped I/O
Option C:	I/O mapped
Option D:	None of the above
Q4.	The _____ address of a memory is a 20 bit address for the 8086 microprocessor.
Option A:	Physical
Option B:	Logical
Option C:	Both
Option D:	None of these
Q5.	The pipelining process is also called as _____

Option A:	Superscalar operation
Option B:	Assembly line operation
Option C:	Von Neumann cycle
Option D:	None of the mentioned
Q6.	Each stage in pipelining should be completed within _____ cycle.
Option A:	1
Option B:	2
Option C:	3
Option D:	4
Q7.	The method which offers higher speeds of I/O transfers is _____
Option A:	Interrupts
Option B:	Memory mapping
Option C:	Program-controlled I/O
Option D:	DMA
Q8.	_____ register is used as a default counter in case of string and loop instructions.
Option A:	AX
Option B:	BX
Option C:	CX
Option D:	DX
Q9.	The periods of time when the unit is idle is called as _____
Option A:	Stalls
Option B:	Bubbles
Option C:	Hazards
Option D:	Both Stalls and Bubbles
Q10.	The instruction “JUMP” belongs to
Option A:	sequential control flow instructions
Option B:	control transfer instructions
Option C:	branch instructions
Option D:	control transfer & branch instructions
Q11.	Operation code field is present in
Option A:	programming language instruction

Option B:	assembly language instruction
Option C:	machine language instruction
Option D:	none of the mentioned
Q12.	In memory-mapped I/O _____
Option A:	The I/O devices and the memory share the same address space
Option B:	The I/O devices have a separate address space
Option C:	The memory and I/O devices have an associated address space
Option D:	A part of the memory is specifically set aside for the I/O operation
Q13.	In order to initiate the fetch cycle by BIU atleast _____ bytes of the queue must be empty
Option A:	1
Option B:	2
Option C:	3
Option D:	4
Q14.	The memory which is used to store the copy of data or instructions stored in larger memories, inside the CPU is called _____
Option A:	Level 1 cache
Option B:	Level 2 cache
Option C:	Registers
Option D:	TLB
Q15.	The situation wherein the data of operands are not available is called _____
Option A:	Data hazard
Option B:	Stock
Option C:	Deadlock
Option D:	Structural hazard
Q16.	A 16-bits address bus can generate _____addresses.
Option A:	32767
Option B:	25652
Option C:	65536
Option D:	None of the mentioned
Q17.	_____ is the permanent memory built into your computer called.
Option A:	ROM
Option B:	CPU

Option C:	DVD-ROM
Option D:	RAM
Q18.	The BIU prefetches the instruction from memory and store them in _____.
Option A:	Queue
Option B:	Register
Option C:	Memory
Option D:	Stack
Q19.	MAR stands for _____
Option A:	Memory address register
Option B:	Main address register
Option C:	Main accessible register
Option D:	Memory accessible register
Q20.	Which of the following is used for binary multiplication?
Option A:	Restoring Multiplication
Option B:	Booth's Algorithm
Option C:	Pascal's Rule
Option D:	Digit-by-digit multiplication
Q21.	Which of the following is often called the double precision format?
Option A:	64
Option B:	8
Option C:	32
Option D:	128
Q22.	If MN/MX is low, the 8086 operates in _____ mode.
Option A:	Minimum mode
Option B:	Maximum mode
Option C:	Both A and B
Option D:	Control mode
Q23.	The IEEE standard followed by almost all the computers for floating point arithmetic _____
Option A:	IEEE 260
Option B:	IEEE 488
Option C:	IEEE 754

Option D:	IEEE 610
Q24.	The number of address and data lines of 8086_____.
Option A:	8 and 8
Option B:	16 and 16
Option C:	20 and 16
Option D:	16 and 20
Q25.	Base Pointer (BP) contains offset address of _____ segment.
Option A:	Data segment
Option B:	Code segment
Option C:	Stack segment
Option D:	Extra segment