University of Mumbai
Examination 2020 under cluster APSIT

Program: Computer Engineering
Curriculum Scheme: Rev2016
Examination: Second Year Semester IV
Course Code: CSC403 and Course Name: Computer Organization and Architecture
Time: 1 hour Max. Marks: 50
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For the students:- All the Questions are compulsory and carry equal marks .

Q1.	Which representation is commonly used by computer?
Option A:	Sign Magnitude representation
Option B:	1's complement representation
Option C:	2's complement representation
Option D:	9's complement representation
Q2.	In IEEE 32-bit representations, the mantissa of the fraction is said to occupy _____ bits.
Option A:	24
Option B:	23
Option C:	20
Option D:	16
Q3.	Which of the following is/are true? a. Computer organization refers to the design of functional blocks in a computer system. b. Computer organization is responsible to integrate functional blocks of a computer system. c. Computer architecture refers to the design of components and functional block of a computer system. d. Computer architecture concerns the integration of various functional blocks to build a computer system.
Option A:	a,d
Option B:	a,b
Option C:	b,c
Option D:	c,d
Q4.	Which architecture is followed by general purpose microprocessors?
Option A:	Harvard architecture
Option B:	Von Neumann architecture
Option C:	PCI Bus
Option D:	ALU
Q5.	The _____ holds the contents of the accessed memory word.

Option A:	MAR
Option B:	MBR
Option C:	PC
Option D:	IR
Q6.	Content of the program counter is added to the address part of the instruction in order to obtain the effective address is called
Option A:	Index addressing mode
Option B:	Implied addressing mode
Option C:	Relative addressing mode
Option D:	Register addressing mode
Q7.	SPEC stands for _____
Option A:	Standard Performance Evaluation Code
Option B:	System Performance Evaluation Corporation
Option C:	System Processing Enhancing Code
Option D:	Standard Processing Enhancement Corporation
Q8.	In a computer based on three-address instruction format, each address field can be used to specify which of the following: (S1) A memory operand (S2) A processor register (S3) An implied accumulator register
Option A:	Either S1 or S2
Option B:	Either S2 or S3
Option C:	Only S2 and S3
Option D:	All of S1, S2 and S3
Q9.	In a micro programmed control unit, micro instructions are stored in special memory called
Option A:	Control memory
Option B:	RAM
Option C:	ROM
Option D:	Micro memory
Q10.	Delay element method uses _____ for control timing signals
Option A:	T flip flop
Option B:	D flip flop
Option C:	SR flip flop
Option D:	JK flip flop
Q11.	The control signals generated for the operation MAR<-PC are
Option A:	PCout, MARin
Option B:	MARin,PCout
Option C:	PCin, MARin
Option D:	PCout, MARout
Q12.	Which of the following statement is false?

Option A:	Hardwired control unit is slower than micro-programmed control unit.
Option B:	Micro programmed control unit is flexible than hardwired control unit
Option C:	State table, Delay Element and Sequence Counter are methods for implementing hardwired control.
Option D:	A sequence of microinstructions constitutes a microprogram
Q13.	A certain processor uses a fully associative cache of size 16 kB. The cache block size is 16 bytes. Assume that the main memory is byte addressable and uses a 32-bit address. How many bits are required for the *Tag* and the *Index* fields respectively in the addresses generated by the processor?
Option A:	24 bits and 0 bits
Option B:	28 bits and 4 bits
Option C:	24 bits and 4 bits
Option D:	28 bits and 0 bits
Q14.	The idea of cache memory is based
Option A:	on the property of locality of reference
Option B:	on the fact that references generally tend to cluster
Option C:	on the heuristic 90-10 rule
Option D:	on the output
Q15.	Which of the following is lowest in memory hierarchy?
Option A:	Cache memory
Option B:	Secondary memory
Option C:	Registers
Option D:	RAM
Q16.	The offset ‘d’ of the logical address must be _____
Option A:	greater than segment limit
Option B:	between 0 and segment limit
Option C:	between 0 and the segment number
Option D:	greater than the segment number
Q17.	If the size of logical address space is 2 to the power of m, and a page size is 2 to the power of n addressing units, then the high order _____ bits of a logical address designate the page number, and the ____ low order bits designate the page offset.
Option A:	m, n
Option B:	n, m
Option C:	m – n, m
Option D:	m – n, n
Q18.	Which of the following statement is false?
Option A:	External fragmentation exists when enough total memory exists to satisfy a request but it is not contiguous
Option B:	When the memory allocated to a process is slightly larger than the process, then internal fragmentation occurs
Option C:	When memory is divided into several fixed sized partitions, each partition may contain exactly one process

Option D:	Segmentation is the concept in which a process is copied into main memory from the secondary memory according to the requirement.
Q19.	The return address from the interrupt-service routine is stored on the----
Option A:	System queue
Option B:	Processor register
Option C:	Processor stack
Option D:	Memory
Q20.	The method which offers higher speeds of I/O transfers is
Option A:	Interrupts
Option B:	Memory mapping
Option C:	Program-controlled I/O
Option D:	DMA
Q21.	The method of accessing the I/O devices by repeatedly checking the status flags is
Option A:	Program-controlled I/O
Option B:	Memory-mapped I/O
Option C:	I/O mapped
Option D:	DMA
Q22.	VLIW stands for:
Option A:	Vector Large Instruction Word
Option B:	Very Long Instruction Word
Option C:	Very Large Integrated Word
Option D:	Very Low Integrated Word
Q23.	Von Neumann architecture is
Option A:	SISD
Option B:	MISD
Option C:	MIMD
Option D:	SIMD
Q24.	The algorithm followed in most of the systems to perform out of order execution is
Option A:	Tomasulo's algorithm
Option B:	Score carding
Option C:	Reader-writer algorithm
Option D:	Banker's Algorithm
Q25.	What is another name of loosely coupled multiprocessor?
Option A:	Distributed memory processors
Option B:	Shared memory processors
Option C:	Mutually coupled processors
Option D:	Binding memory processors