

**University of Mumbai**  
**Examination 2020 under cluster APSIT**

Program: Computer Engineering

Curriculum Scheme: Rev2016

Examination: Second Year Semester III

Course Code: CSC302 and Course Name: Digital Logic Design & Analysis

Time: 1 hour

Max. Marks: 50

For the students: - All the Questions are compulsory and carry equal marks.

Q1.	The decimal equivalent of the binary number $(1011.011)_2$ is _____
Option A:	$(11.375)_{10}$
Option B:	$(10.123)_{10}$
Option C:	$(11.175)_{10}$
Option D:	$(9.23)_{10}$
Q2.	The representation of octal number $(532.2)_8$ in decimal is _____
Option A:	$(346.25)_{10}$
Option B:	$(532.864)_{10}$
Option C:	$(340.67)_{10}$
Option D:	$(531.668)_{10}$
Q3.	Any signed negative binary number is recognized by its ____
Option A:	MSB
Option B:	LSB
Option C:	Nibble
Option D:	Word
Q4.	Convert the hexadecimal number $(1E2)_{16}$ to decimal:
Option A:	480
Option B:	483
Option C:	482
Option D:	484
Q5.	What is the addition of the binary numbers 11011011010 and 010100101?
Option A:	0111001000
Option B:	1100110110
Option C:	11101111111
Option D:	10011010011
Q6.	The logical sum of two or more logical product terms is called _____
Option A:	SOP
Option B:	POS
Option C:	OR Operation
Option D:	NAND Operation
Q7.	The expression $Y=(A+B)(B+C)(C+A)$ shows the _____ operation
Option A:	SOP
Option B:	POS

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Option C:	XOR
Option D:	NOR
Q8.	A product term containing all K variables of the function in either complemented or uncomplemented form is called a _____
Option A:	Minterm
Option B:	Maxterm
Option C:	Midterm
Option D:	$\Sigma$ term
Q9.	The prime implicant which has at least one element that is not present in any other implicant is known as _____
Option A:	Essential Prime Implicant
Option B:	Implicant
Option C:	Complement
Option D:	Prime Complement
Q10.	Don't care conditions can be used for simplifying Boolean expressions in _____
Option A:	Registers
Option B:	Terms
Option C:	K-maps
Option D:	Latches
Q11.	The output of an EX-NOR gate is 1. Which input combination is correct?
Option A:	A = 1, B = 0
Option B:	A = 0, B = 1
Option C:	A = 0, B = 0
Option D:	A = 0, B' = 1
Q12.	The number of full and half adders are required to add 16-bit number is _____
Option A:	8 half adders, 8 full adders
Option B:	1 half adders, 15 full adders
Option C:	16 half adders, 0 full adders
Option D:	4 half adders, 12 full adders
Q13.	How many full adders are required to construct an m-bit parallel adder?
Option A:	m/2
Option B:	m
Option C:	m-1
Option D:	m+1
Q14.	The code where all successive numbers differ from their preceding number by single bit is _____
Option A:	Alphanumeric Code
Option B:	BCD
Option C:	Excess 3
Option D:	Gray

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Q15.	A universal logic gate is one which can be used to generate any logic function. Which of the following is a universal logic gate?
Option A:	OR
Option B:	AND
Option C:	XOR
Option D:	NAND
Q16.	A counter circuit is usually constructed of _____
Option A:	A number of latches connected in cascade form
Option B:	A number of NAND gates connected in cascade form
Option C:	A number of flip-flops connected in cascade
Option D:	A number of NOR gates connected in cascade form
Q17.	What is the maximum possible range of bit-count specifically in n-bit binary counter consisting of 'n' number of flip-flops?
Option A:	0 to $2^n$
Option B:	0 to $2^n + 1$
Option C:	0 to $2^n - 1$
Option D:	0 to $2^{n+1/2}$
Q18.	Ripple counters are also called _____
Option A:	SSI counters
Option B:	Asynchronous counters
Option C:	Synchronous counters
Option D:	VLSI counters
Q19.	BCD counter is also known as _____
Option A:	Parallel counter
Option B:	Decade counter
Option C:	Synchronous counter
Option D:	VLSI counter
Q20.	A register is defined as _____
Option A:	The group of latches for storing one bit of information
Option B:	The group of latches for storing n-bit of information
Option C:	The group of flip-flops suitable for storing one bit of information
Option D:	The group of flip-flops suitable for storing binary information
Q21.	Registers capable of shifting in one direction is _____
Option A:	Universal shift register
Option B:	Unidirectional shift register
Option C:	Unipolar shift register
Option D:	Unique shift register
Q22.	A shift register is defined as _____
Option A:	The register capable of shifting information to another register
Option B:	The register capable of shifting information either to the right or to the left

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Option C:	The register capable of shifting information to the right only
Option D:	The register capable of shifting information to the left only
Q23.	The full form of SIPO is _____
Option A:	Serial-in Parallel-out
Option B:	Parallel-in Serial-out
Option C:	Serial-in Serial-out
Option D:	Serial-In Peripheral-Out
Q24.	Which combinational circuit is renowned for selecting a single input from multiple inputs & directing the binary information to output line?
Option A:	Data Selector
Option B:	Data distributor
Option C:	Both data selector and data distributor
Option D:	DeMultiplexer
Q25.	Which is the major functioning responsibility of the multiplexing combinational circuit?
Option A:	Decoding the binary information
Option B:	Generation of all minterms in an output function with OR-gate
Option C:	Generation of selected path between multiple sources and a single destination
Option D:	Encoding of binary information