University of Mumbai
Examination 2020 under cluster 5 (APSIT)

Program: BE Computer Engineering

Curriculum Scheme: Revised 2016

Examination: Third Year Semester V

Course Code: CSC501 and Course Name: Microprocessor

Time: 1 hour Max. Marks: 50

==========

Note to the students:- All the Questions are compulsory and carry equal marks .

Q1.	In which T-state does the CPU sends the address to memory or I/O and the ALE signal for demultiplexing _____.
Option A:	T1
Option B:	T2
Option C:	T3
Option D:	T4
Q2.	Intel 8288 is a bus controller designed for Intel _____.
Option A:	IC 8086 Min Mode
Option B:	IC 8086 Max Mode
Option C:	IC 8008
Option D:	IC 8259 PIC
Q3.	A segment starts at a particular address and its maximum size can go up to 64kilobytes. But if another segment starts along with this 64 kilobytes location of the first segment, then the two are said to be_____.
Option A:	memory segment
Option B:	Stack segment
Option C:	Data segment
Option D:	Overlapping Segment
Q4.	Which of the following flag is not a control flag register of IC 8086
Option A:	Directional flag
Option B:	Overflow flag
Option C:	Trap flag
Option D:	Interrupt flag
Q5.	Which is not part of the execution unit of 8086 microprocessor
Option A:	Arithmetic logics unit
Option B:	Clock
Option C:	general register
Option D:	flag

Q6.	Which one is not a string instruction?
Option A:	MOVS
Option B:	STOS
Option C:	STRS
Option D:	CMPS
Q7.	Assume BL = FF INC BL will give output as :
Option A:	BL= FE
Option B:	BL= 00
Option C:	BL= 01
Option D:	BL= 11
Q8.	ADD BL, 25H is an example of which addressing mode?
Option A:	Immediate addressing mode
Option B:	Implied addressing mode
Option C:	Direct addressing mode
Option D:	Indirect addressing mode
Q9.	Implied addressing refers to:
Option A:	instructions that comprise an opcode with an operand
Option B:	instructions that comprise an opcode with multiple operands
Option C:	instructions that comprise only an opcode without an operand
Option D:	No such addressing mode exists.
Q10.	The Loop instructions use ____ register to indicate the loop count
Option A:	AX
Option B:	BX
Option C:	CX
Option D:	DX
Q11.	The _____ determines the priorities of the bits set in the IRR
Option A:	IMR
Option B:	ISR
Option C:	Priority Resolver
Option D:	Memory
Q12.	Which Register in 8259 PPI stores all the levels that are currently being serviced.
Option A:	IMR
Option B:	ISR
Option C:	IRR
Option D:	Priority Resolver
Q13.	An interrupt caused by an external signal is referred as.

Option A:	Maskable Interrupt
Option B:	Software Interrupt
Option C:	Hardware Interrupt
Option D:	Non Maskable Interrupt
Q14.	How Many INTA pulse send by microprocessor to 8259 PPI
Option A:	Three
Option B:	Two
Option C:	None
Option D:	One
Q15.	In 8255, under the I/O mode of operation we have __ modes. Under which mode will have the following features: A 5 bit control port is available. Three I/O lines are available at Port C.
Option A:	3, Mode2
Option B:	2, Mode 2
Option C:	4, Mode 3
Option D:	3, Mode 2
Q16.	The number of clock cycles required for an 8257 to complete a transfer is
Option A:	2
Option B:	4
Option C:	8
Option D:	1
Q17.	In which of the following modes of the 8255 PPI, only port C is taken into consideration?
Option A:	3
Option B:	Mode 0 of I/O mode
Option C:	Mode 1 of I/O mode
Option D:	Mode 2 of I/O mode
Q18.	DMA stands for
Option A:	Direct memory access
Option B:	Direct memory allocation
Option C:	Data memory access
Option D:	Data memory allocation
Q19.	Which mode of 8253 can provide pulse width modulation?
Option A:	programmable one-shot
Option B:	square wave rate generator
Option C:	software triggered strobe

Option D:	hardware triggered strobe
Q20.	How many bits are provided for IOPL flag in EFLAG register of 80386 microprocessor?
Option A:	1
Option B:	2
Option C:	16
Option D:	32
Q21.	In 80386, Size of linear address is ……
Option A:	8
Option B:	16
Option C:	32
Option D:	48
Q22.	In 80386, Size of LDTR is ……
Option A:	8 bits
Option B:	16 bits
Option C:	32 bits
Option D:	48 bits
Q23.	In Pentium Integer pipeline has …. stages.
Option A:	2
Option B:	4
Option C:	5
Option D:	8
Q24.	How many of bits are allocated for history in branch prediction logic?
Option A:	2
Option B:	4
Option C:	8
Option D:	16
Q25.	Branch is predicted in …… stage of Integer pipeline of Pentium.
Option A:	D1 (Decode 1)
Option B:	D2 (Decode 2)
Option C:	EX (Execute)
Option D:	WB (Write back)