Program: BE Computer Engineering

Curriculum Scheme: Revised 2012

Examination: Third Year Semester V

Course Code: CPC501 and Course Name: Microprocessor

Time: 1 hour Max. Marks: 50

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Note to the students:- All the Questions are compulsory and carry equal marks .

Q1.	IP is a 16-bit register. It holds offset of the next instructions in the _____.
Option A:	Code segment
Option B:	data segment
Option C:	stack segment
Option D:	extra segment
Q2.	8086 generates the 20-bit physical address using Segment and Offset addresses using the formula: Physical Address = _____*10H + offset Address.
Option A:	Logical address
Option B:	Segment address
Option C:	Data address
Option D:	Memory address.
Q3.	In which T-state does the CPU sends the address to memory or I/O and the ALE signal for demultiplexing _____.
Option A:	T1
Option B:	T2
Option C:	T3
Option D:	T4
Q4.	A segment starts at a particular address and its maximum size can go up to 64kilobytes. But if another segment starts along with this 64 kilobytes location of the first segment, then the two are said to be_____.
Option A:	memory segment
Option B:	Stack segment
Option C:	Data segment
Option D:	Overlapping Segment
Q5.	IC 8284 Clock generator is a _____ pin chip.
Option A:	20

Option B:	18
Option C:	40
Option D:	32
Q6.	Which of the following is not an arithmetic instruction?
Option A:	INC
Option B:	CMP
Option C:	DEC
Option D:	ROL
Q7.	The Loop instructions use ____ register to indicate the loop count
Option A:	AX
Option B:	BX
Option C:	CX
Option D:	DX
Q8.	Assume AL= 0011 0101 NEG AL will give what output?
Option A:	AL = 1011 0101
Option B:	AL = 1100 1010
Option C:	AL = 1100 1011
Option D:	AL = 1111 1111
Q9.	Which one is not a string instruction?
Option A:	MOVS
Option B:	STOS
Option C:	STRS
Option D:	CMPS
Q10.	Instruction prefix REP is used
Option A:	to identify 8087 instructions
Option B:	to lock the system bus during an instruction
Option C:	to repeatedly execute string instructions
Option D:	to repeatedly fetch the data
Q11.	PIC can deal with maximum up to _____ interrupt inputs
Option A:	8
Option B:	64
Option C:	16
Option D:	32
Q12.	Type 3 interrupt is
Option A:	Single Step Interrupt
Option B:	Overflow Interrupt
Option C:	Break Point Interrupt
Option D:	Divide by Zero Interrupt

Q13.	In 8257 (DMA), each of the four channels has
Option A:	a pair of two 8-bit registers
Option B:	a pair of two 16-bit registers
Option C:	one 8-bit register
Option D:	one 32-bit register
Q14.	The 8259 can set up as a master or a slave by _____ pin
Option A:	SP/ EN
Option B:	IMR
Option C:	INT
Option D:	ISR
Q15.	ICW 3 is used when there are _____
Option A:	More than one 8259 available
Option B:	Only one 8259 available
Option C:	multiple INTR available
Option D:	Non maskable interrupt available
Q16.	Which microprocessor pins are used to request and acknowledge a DMA transfer?
Option A:	Ready and Wait
Option B:	Reset and Wait
Option C:	INTR and INTA
Option D:	HOLD and HLDA
Q17.	In 8255, under the I/O mode of operation we have __ modes. Under which mode will have the following features: A 5 bit control port is available. Three I/O lines are available at Port C.
Option A:	3, Mode2
Option B:	2, Mode 2
Option C:	4, Mode 3
Option D:	3, Mode 2
Q18.	The number of counters that are present in the programmable timer device 8254 is
Option A:	1
Option B:	2
Option C:	3
Option D:	4
Q19.	Which mode of 8253 can provide pulse width modulation?
Option A:	programmable one-shot

Option B:	square wave rate generator
Option C:	software triggered strobe
Option D:	hardware triggered strobe
Q20.	In which of the following modes is the 8255 PPI capable of transferring data while handshaking with the interfaced device?
Option A:	BSR mode
Option B:	Mode 0 of I/O mode
Option C:	Mode 1 of I/O mode
Option D:	Mode 2 of I/O mode
Q21.	The programmable timer device (8253) contains three independent _____ bit counters.
Option A:	8
Option B:	16
Option C:	20
Option D:	32
Q22.	In 80386, Size of LDTR is ……
Option A:	8 bits
Option B:	16 bits
Option C:	32 bits
Option D:	48 bits
Q23.	In protected mode of 80386, size of memory page is ….
Option A:	1 KB
Option B:	4 KB
Option C:	8 KB
Option D:	1 MB
Q24.	Branch is predicted in …… stage of Integer pipeline of Pentium.
Option A:	D1 (Decode 1)
Option B:	D2 (Decode 2)
Option C:	EX (Execute)
Option D:	WB (Write back)
Q25.	In Pentium Floating point pipeline has …. stages.
Option A:	2
Option B:	4
Option C:	5
Option D:	8